Sleepy Stack Approach for Low Power P Flip Flop

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Abstract—In today’s world power dissipation has become one of the most important criteria for selection and implementation of any microelectronics circuit. The need for low power has caused a major epiphenomenal shift where the power dissipation is critical factor as most of the devices are battery operated. There are two fundamental components which determine the power consumption these are static and dynamic power. Static power consumption is a major concern in VLSI technologies. As the technology is scaling down and higher operating speeds of CMOS VLSI circuits, the leakage power is also getting increased. The consumption of power has to be reduced without affecting the normal operation of the system with considering the corresponding speed and area trade-off. In this proposed work the power dissipation during inactive (standby) mode of operation is compared between stack, sleep and sleepy stack method. The proposed design techniques are applied to a low power pulse triggered flip flop. The circuits are designed and simulated using Tanner EDA tool using 18 nm technology files.

Keywords— Leakage Power, Standby, Sleep, Stack, Sleepy Stack.

I. Introduction

Power consumption is one of the most important aspect of VLSI circuit design. The focus of designers is on low power design because of huge growing demands of portable applications. To solve the problem for dissipation of power, many researchers have given different ideas from device to the architectural level. But there is no universal way to completely mask the trade-offs between power, delay and area associated with the VLSI designs [16]. So it is very essential to keep the perfect balance between these three pillars. With the advance in the VLSI technology, the channel length, oxide thickness and threshold voltage of transistor is reducing. This reduction in transistor parameters enhances the leakage current in nonlinear fashion. As per International Technology Roadmap for Semiconductor (ITRS) “leakage current is going to be a major factor limiting this successive scaling down of transistors” [1]. Because of the smaller feature size, the channel length is also very small which leads to increase in the sub-threshold current of transistor in the off state. The lower threshold voltage ($V_{th}$) gives rise to increase in sub-threshold current as transistors does not get switched off completely. Due to increase in the successive technology, the density of transistors is also increasing this leads to non-linear increase in the leakage power. So it is very important to develop design techniques to reduce the dissipation of static power during idle state of the circuit or device. This technique of power reduction should be such that it should not affect the normal function of the system. So developing
such technique keeping normal function (logic) unaffected is a big challenge. A technique called as sleepy stack is efficient solution to above problem. In this paper all three methods i.e. sleep, stack, sleepy stack are applied to p flip-flop and significant reduction in leakage power is achieved.

II. Design of Low Power P - Flip Flop

Flip-flops (FFs) are the fundamental storage elements used in all kinds of digital designs. Nowadays the digital designs adopts intensive pipelining techniques which employs many FF rich modules such as shift register, register file, first in first out (FIFO). It is also estimated that the consumption of power by the clock system consisting of clock distribution networks and FFs, is as high as 50% of the total power of consumed by the system [7]. Hence FFs contributes substantial portion of the chip area and power consumption to the overall design of the system [16], [17]. Pulse-triggered Flip Flop (P-FF) is more popularly used than the conventional master–slave and transmission gate based FFs because of its single-latch structure in high-speed and low power applications [2]. As in P-FF, only one latch is required a P-FF is simpler in complexity of circuit. This leads to faster toggle rate for high speed operations. The p flip flop also allow time lending across the clock cycle corners and hence provides zero or even negative setup time. Despite these advantages of P-FF pulse generation requires crucial pulse width control to overcome the possible variations in process technology and in signal distribution network.

The figure 6 shows the P –FF with stack transistor with improved structure implemented with stack transistor. In this design we have used single stacking only at GND by experimental result we analysed that putting stack transistors at VDD and GND gives same reduction in power as that of in the case of putting it at foot. In the stack technique as the W/L ratio of transistor is made half it increases the threshold voltage and by cascading two transistors in series the effective threshold voltage of stack transistors increase by very high value [8],[12]. This is the main principle behind...
reduction in leakage power in stack transistors. By this implementation there is reduction in active power by 3.48 times and in standby by 23.22 times than in the normal P flip flop.

2. P - Flip Flop with Sleep transistor

![Fig.7 - P Flip Flop with sleep transistor technique](image)

The figure 7 shows the P –FF with improved structure implemented with sleep transistor. In this design we have used sleep transistors only at GND by experimental result we analysed that putting sleep transistors at VDD and GND gives same reduction in power as that of in the case of putting it at foot. The sleep signal is explicitly provided externally. It is observed that sleep transistor technique provides better reduction than in stack transistor technique but only disadvantage is that external sleep signal need to provide and a delay occurs because it takes time enter and exit in the sleep mode safely [5] [6]. By this implementation there is reduction in active power by 2.12 times and in standby by 32.75 times than in the normal P flip flop.

3. P - Flip Flop with Sleepy Stack transistor

![Fig.8 - P flip flop with sleepy stack transistor technique](image)

The figure 9 shows the P –FF with sleepy stack transistor. The Sleepy-Stack technique is more efficient than sleep and stacks technique as it takes the advantages of both sleep and stack technique for the reduction of leakage current flowing through off transistors [9]. By this implementation there is reduction in active power by 1.56 times and in standby by 60 times than in the normal P flip flop.

IV. SIMULATION RESULTS

The focus of the paper is on the the analysis of reduction in power dissipation of sleepy stack approach with respect to its fundamental sleep and stack technique. The work is done to analysed the power in active as well as inactive i.e. in idle mode.

![Fig.9 - Statistical analysis of different leakage power dissipation techniques](image)

Fig.9 shows statistical analysis of different techniques of leakage power reduction used in this paper. The first is simple i.e. normal P- FF in which no power reduction technique is used. From experimental results it is clear that sleepy stack technique is very efficient for reducing the leakage power reduction as it reduces as high as 60 times that takes place in normal P-FF. For the implementation of the proposed work we have used Tanner EDA tool in 18nm technology file at the operating temperture of 25 degree celcius.
Evaluation of different low power techniques

Table 1- Power dissipation in Active mode.

<table>
<thead>
<tr>
<th>ACTIVE POWER</th>
<th>Maximum Power</th>
<th>Minimum Power</th>
<th>Average Power</th>
</tr>
</thead>
<tbody>
<tr>
<td>P-FF [Simple]</td>
<td>$1.975e^{-5}$</td>
<td>$2.12e^{-7}$</td>
<td>$1.975e^{-5}$</td>
</tr>
<tr>
<td>P-FF [Stack]</td>
<td>$3.18e^{-5}$</td>
<td>$3.70e^{-7}$</td>
<td>$1.395e^{-6}$</td>
</tr>
<tr>
<td>P-FF [Sleep]</td>
<td>$4.64e^{-3}$</td>
<td>$2.123e^{-7}$</td>
<td>$8.80e^{-6}$</td>
</tr>
<tr>
<td>P-FF [Sleepy Stack]</td>
<td>$3.18e^{-5}$</td>
<td>$3.65e^{-7}$</td>
<td>$3.44e^{-6}$</td>
</tr>
</tbody>
</table>

Table 2- Power dissipation in Inactive (Idle) mode.

<table>
<thead>
<tr>
<th>INACTIVE POWER</th>
<th>Maximum Power</th>
<th>Minimum Power</th>
<th>Average Power</th>
</tr>
</thead>
<tbody>
<tr>
<td>P-FF [Simple]</td>
<td>$3.3e^{-3}$</td>
<td>$3.27e^{-3}$</td>
<td>$3.27e^{-3}$</td>
</tr>
<tr>
<td>P-FF [Stack]</td>
<td>$9.497e^{-7}$</td>
<td>$4.0e^{-7}$</td>
<td>$7.69e^{-7}$</td>
</tr>
<tr>
<td>P-FF [Sleep]</td>
<td>$5.97e^{-5}$</td>
<td>$6.045e^{-9}$</td>
<td>$5.45e^{-7}$</td>
</tr>
<tr>
<td>P-FF [Sleepy Stack]</td>
<td>$3.18e^{-5}$</td>
<td>$1.03e^{-18}$</td>
<td>$2.988e^{-7}$</td>
</tr>
</tbody>
</table>

V. CONCLUSION

In nanometer scale CMOS technology, sub threshold leakage power dissipation is a big challenge. The VLSI designers choose reduction techniques based on the technology to be used and design criteria to be fulfilled. In this paper, we have provided comparison between P flip flop implemented by sleep, stack and sleepy stack method. This work is done in order to find the reduction of power in sleep, stack and their combination sleepy stack technique. It is found that sleepy stack technique takes the advantages of both sleep and stack techniques and gives as high as 60 times reduction in leakage power dissipation than the normally operated pulse triggered flip flop in the inactive (idle) mode.

REFERENCES


